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Design And Implementation Of QPSK Modulation System

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Abstract : **Quadrature Phase Shift Keying (QPSK) is one of the most popular digital modulations. The QPSK modulator consumes less power and bandwidth in a modern devices but for a system like satellite and mobile devices where their operations are power limited, this is a problem that needs to be fixed. The objective is to design the QPSK modulator that uses less power for operation and it should be bandwidth efficient. Although, this process may seem to be insignificant at initial stage, but this modulation scheme enables the carrier to transmit the 2-bits of information instead of 1-bit. This doubling makes the bandwidth of the carrier, more effective. The proposed modulator successfully modeled with Verilog Hardware Description Language (HDL), simulated with Xilinx Integrated Software Environment (ISE) version 14.5 software. QPSK modulation is also performed on MATLAB tool.**

Keywords—Verilog, QPSK, PHASE, MATLAB, Communication.

I.NTRODUCTION

In Communication System we have two main resources. These are the transmission power and the channel bandwidth. The channel bandwidth depends upon the bit rate or signalling rate .In digital bandpass transmission, we use a carrier for transmission. This carrier is transmitted over a channel. If two or more bits are combined in some symbols, then the signalling rate is reduced. This reduces the transmission channel bandwidth. Hence ,because of grouping of bits in symbols, the transmission channel bandwidth is reduced. In quadrature phase shift keying, two successive bits in the data sequence are grouped together. This reduces the bits rate of signalling rate and hence reduces the bandwidth of the channel. In QPSK,two successive bits are combined.This combination of two bits forms four distinct symbols. When the symbol is changed to next symbol the phase of the carrier is changed by 45°. Corresponding phase shifts and symbols in QPSK signal

GENERATION OF QPSK:

A QPSK signal can be generated by independently modulating two carriers in quadrature (cos Zt and sin Zt),
The Serial to Parallel Converter groups the incoming data into di bits (groups of two consecutive bits). Each time two bits have been clocked serially into its buffer, the Serial to Parallel Converter outputs one di bit in parallel at its two outputs. One bit of each di bit is sent to the I channel of the modulator; the other bit is sent to the Q channel of the modulator. Each channel of the modulator works independently to processes the stream of bits it receives. The starting point for grouping bits into di bits is *completely arbitrary*. For educational purposes, the Serial to Parallel Converter in the QPSK application has a **Drop 1 Bit button**. Clicking this button causes the Serial to Parallel Converter to ignore one bit in the data sequence. This changes the grouping of all subsequent data bits into di bits.

The Level Converter in each channel converts the data into a (baseband) bipolar pulse stream that can be applied to one input of the mixer. To restrict the bandwidth of the QPSK signal, a Low-Pass Filter is usually used before the mixer in each channel of the modulator in order to provide the desired spectral shaping. In addition, a bandpass filter (not shown in Figure 5) may be used to filter the QPSK signal before transmission. Quadrature Phase Shift Keying is a modulation technique which is widely used in wireless communication system due to its ability to transmit twice the data rate for a given bandwidth. Even though the QPSK modulator consumes less power in a present devices but for a system such as satellite and mobile devices where their operations and power limited.Wireless communication systems require high data rate for efficient transmission of information. Modulation techniques have been introduced to increase the efficiency in data transmitting and receiving rate modulation method used in communication system is Quadrature Phase ShiftKeying (QPSK), which is one of the form of Phase Shift Keying (PSK) modulation scheme.

The digital method was chosen due to its advantages of digital solutions are apparent. Some of the main advantages of the digital solution are repeatability, cost and the simpler reconfiguration when compared with analog solutions. In QPSK modulation, the carrier phase takes four discrete states that are used to indicate a group of two input data bits. Each group takes one of the QPSK states i.e. ±45º and ±135º

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II. QPSK MODULATOR EQUATION

Principle of QPSK modulation – In Quadrature Phase Shift Keying (QPSK), the information is send by changing the phase of the carrier wave. As the name itself describe (quadrature) means four different possible phases. Making a possible to send the different four every symbol. In Quadrature Phase Shift Keying (QPSK) process either sine or cosine are taken as a basic function for modulation. Modulation is achieved by changing the phase of sin and cosine wave with respect to message signal. The basic equation for QPSK modulation techniques is given below

$$S_{qpsk}(t) = \sqrt{\frac{2E_s}{T_S}} cos\left(2\pi f_c t + (2n-1)\frac{\pi}{4}\right),$$

$$n = 0,1,2,3$$

Where n=1, the phase shift is 45 degrees. The constellation diagram for/4 QPSK is show in fig-1. Here, In constellation diagram has to axes that is x and y axis,which means that the modulated the QPSK signal will have two phase that is an in-phase (I) and quadrature-phase (Q).01,00,10,11 are the four phase of QPSK modulator signal.The fig-2 show the basic block diagram of QPSK modulator.

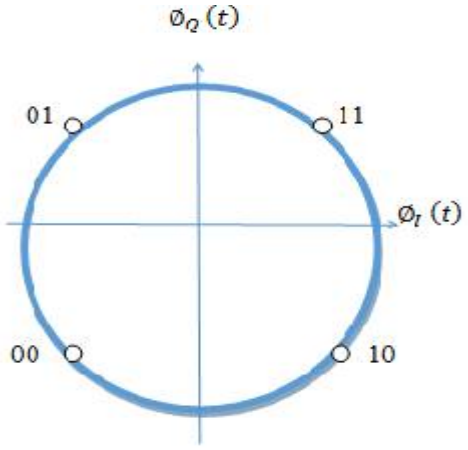

Fig-1 Constellation diagram of QPSK

III. GENERATION OF A QPSK SIGNAL

Figure below shows the mathematical implementation of QPSK[1].

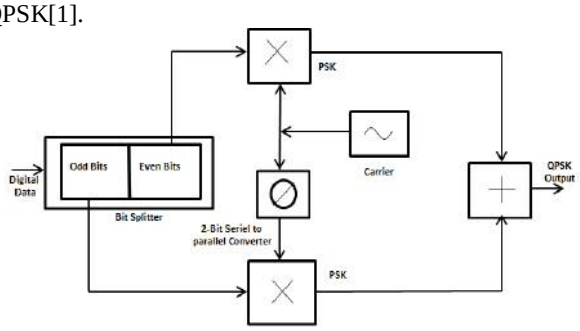

Fig.2.QPSK Block Diagram

Where the first bit represents In-phase (I) and the second bit represent the Quadrature-phase(Q). QPSK modulation is a pair of binary PSK [BPSK], but the data transmission in QPSK is twice when compared to BPSK. The Bit Error Rate (BER) over Signal-to-Noise ratio (SNR) for both the modulation schemes is same. The two BPSK signals are added to produce the required QPSK signal. Since two bit information is transmitted in an interval T, the symbol period for QPSK is two times the bit period i.e. T=2Tb, while for BPSK the symbol period is same as bit period T=Tb. The QPSK signal utilizes half the bandwidth of BPSK signal which consumes low throughput and also has the complexity in hardware implementation [2][4].

The basic idea behind QPSK exploits the fact that cos (2πfct) and sin (2πfct) are orthogonal over the interval [0, Tb] when fc = k/Tb, k integer. Just as in analog modulation, this can be used to transmit two different messages over the same frequency band.[3]. At the input of the modulator, the Bernoulli binary generator is used as a data source which generates random data stream, then the data stream is applied to serial to parallel converter. digital data's are split into even bits (i.e., bits 0,2,4 and so on) and odd bits (i.e.,bits 1,3,5 and so on) are stripped from the data stream by a "bit-splitter" and are multiplied with a carrier to generate a BPSK signal (called PSKI). At the same time, the data's odd bits (i.e., bits 1, 3, 5 and so on) are stripped from the data stream and are multiplied with the same carrier to generate a second BPSK signal (called PSKQ).

IV PROPOSED.IMPLEMENTATION

1) QPSK modulator: The working of QPSK modulator is as follows. The very first block is serial to parallel converter which is also known as demultiplexer. The multiplier takes a

signal and separate even bits and odd bits from generated information bits.

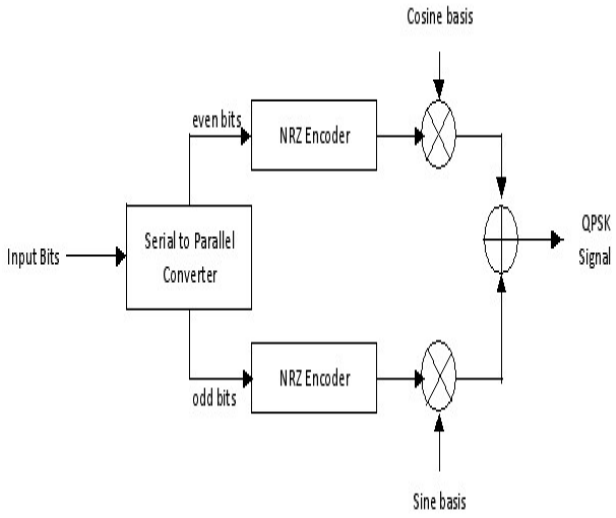

Fig.3. proposed Qpsk block diagram

$$S_{QPSK}(t) = \sqrt{\frac{2E_s}{T_S}} cos(2\pi f_c t) cos\left((2n - 1)\frac{\pi}{4}\right)$$

$$- \sqrt{\frac{2E_s}{T_S}} sin(2\pi f_c t) sin\left((2n-1)\frac{\pi}{4}\right), n = 0,1,2,3$$

The signal is separated into I-phase and Q-phase. The separated odd bits are in quadrature- phase and even bits are in –phase

$$S_{QPSK}(t) = \sqrt{E_S}\, cos\left((2n-1)\frac{\pi}{4}\right) \varphi_I(t) -$$

$$\sqrt{E_S}\, sin\left((2n-1)\frac{\pi}{4}\right) \varphi_Q(t), \quad n=0,1,2,3$$

Then, these odd bits and even bits goes to separate NRZ (non return to zero) encoder .Then the output of both encoder goes to two separate multiplexer ,where it mixed with carrier wave generated by DDS. Basically DDS produced sine and cosine as separate carrier wave with same frequency. Then output NRZ encoder which contains in-phase signal is multiplied by cosine wave and the output of NRZ encoder which contains odd bits is multiplied by sine wave .Then the output of each multiplexer both goes to adder . Where in-phase and Q- phase is added and we get a single signal of 256 samples. There are separated in I-phase and Q-phase as given in below.

$$\varphi_I(t) = \sqrt{\frac{2}{T_S}} cos(2\pi f_c t),$$

$$0 \leq t \leq T, \quad for\ 1$$

-(4)

$$\varphi_Q(t) = \sqrt{\frac{2}{T_S}} sin(2\pi f_c t), \quad 0 \leq t \leq T, \quad for\ 0$$

The four phases $\pi/4, 3\pi/4, 5\pi/4$and **7π/4** as needed. Where n=0,1,2,3 (no of phases) and E_S is signal energy transmitted per symbolis symbol time and frequency of carrier signal,.There are separated in I-phase and Q-phase.

However, the QPSK signal's carrier is phase shifted by before being modulated [1]. The qpsk modulator is designed and simulated using Matlab/Simulink environment and System generator, modulator algorithm has implemented using Verilog hardware description language Xilinx ISE design suite.

V SIMULATON RSULTS

First we have simulated basic QPSK modulator in MATLAB . Then, after output of QPSK modulator is divided into four different phases and these four phases stored in four different ROMs.These four phases modeled with Verilog and simulated on Xilinx ISE 14.4 platform. Now after this we have calculated RTL, timing summary [fig 6.7]. The simulator is used to produce the binary or decimal data and also analog signal to plot the waveforms

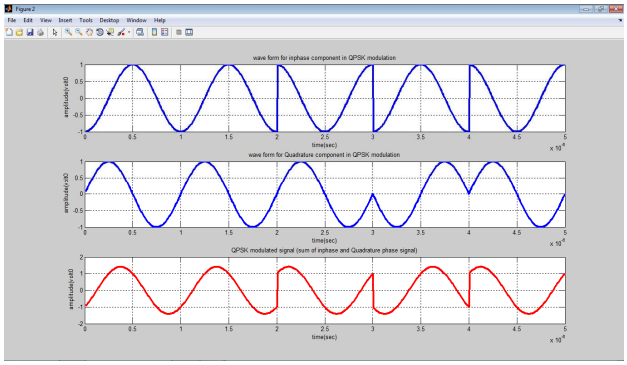

Fig 4. QPSK Carrier Generation

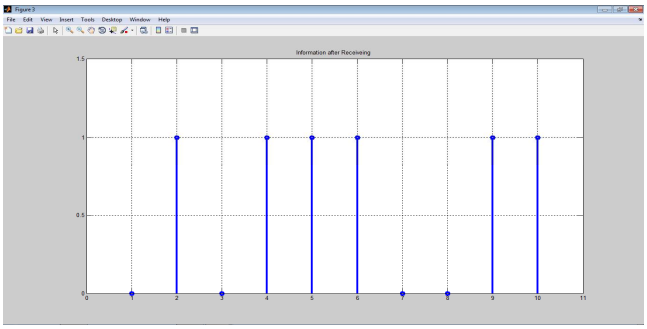

Fig 5. QPSK Modulated Output.

Memory element ROM which is equivalent to input signal either s1(t) or s2(t),provides a sampled data stream that represents the carrier that would normally be generated at the transmitter. The PN generator simulates input data that come from the information source at the transmitter end of the system. A two's complement circuit generates a sampled data stream that represents the modulated carrier that comes from the sending end of the system. The two's complement circuit creates the carrier sampled data phase inversion when the PN signal indicates phase inversion. The sample carrier from ROM and the pseudorandom data pattern are given to two's complement circuit which generates sampled data, representing a received ,modulated carrier signal. If the input data is 1,the phase of the signal is unchanged, but if it is 0,the two's complement circuit yields a phase shift of the transmitted signal.

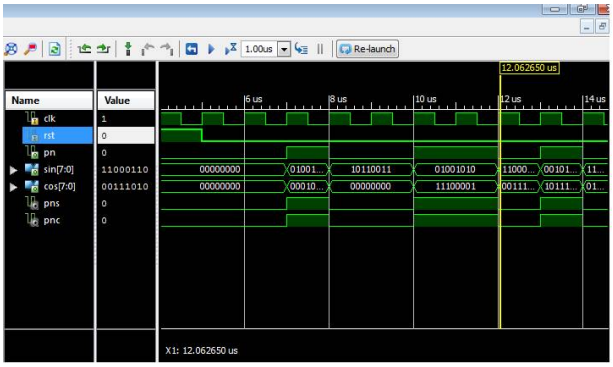

Fig 6. QPSK Modulated output

VI.CONCLUSION

In this technique the four phases of QPSK modulator collected individually and stored in four different ROM. So, proposed method doesn't use mulltiplier, adder, subtractor and DDS, hence high throughput is achieved. In this technique we design QPSK wave for the first time and after that it is processed again and from ROM. So ,there is no need of designing waveform again because of ROM storage, hence time and power is save or we can say less utilized which result in high throughput.

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