A new topology Based 13-Level inverter with various PWM Techniques

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Abstract: When contrasted with routine inverter topologies like diode clasped and capacitor cinched inverters, the cascaded multilevel inverter has lesser music and also lower switching stress. The fell topology has more number of power changes prompting more prominent warmth misfortunes, bigger size, higher cost and more door drive hardware. The proposed configuration contains less number of switches and creates lesser harmonics in the yield voltage than the fell topology. A comparison between four distinct sorts of heartbeat width regulation (PWM) techniques, to be specific, In-stage mien (IPD), Anti-phase disposition (APD), Carrier Overlap (CO) and Variable Frequency (VF) PWM strategies, has been finished. The outcomes have been checked through reproduction contemplate in MATLAB/Simulink in order to choose the best PWM technique that gives minimum THD in the yield voltage. A LC channel has been outlined to improve the consonant profile.

Index Terms— Multilevel inverter, PWM procedure, add up to harmonic distortion, LC channel.

I. INTRODUCTION

Control electronic gadgets assume a noteworthy part in the conversion and control of electric power, particularly to extract power from renewable vitality sources like photovoltaic array and wind vitality [1]. Transformation of DC to AC power can be done with the assistance of inverters (single stage or three phases). Conventional bipolar inverters deliver rotating staircase waveforms with higher music. Hence, the multilevel inverters (MLI) were produced [2]. This paper gives over again three stage design to create the II-level output with less aggregate symphonious mutilation (THD) in its yield voltage. IPD, APD, CO and VF PWM procedures were accustomed to produce switching pulses[3]. The fell H-connect (CHB) design has lesser number of parts when contrasted with the conventional diode braced or capacitor clasped inverters [4]. It contains single stage inverters associated in arrangement with isolated DC sources that can be gotten from renewable vitality sources like sun powered PV cell, bio energy component or wind turbine [5]. Each single phase inverter produces two DC voltage levels. Spans with separate DC sources are fell to each other for more DC levels. The switches work at principal recurrence of 50Hz.

The diode cinched MLI has 20 switches, 90 diodes and 10 primary DC-transport capacitors per stage to deliver a 11-level staircase as the yield voltage. The capacitor clamped MLI utilizes 20 switches, 45 bracing capacitors and 10 main DC-transport capacitors per stage though the fell H-bridge inverter utilizes just 24 changes for each stage to deliver the same yield [6-7]. This paper portrays a solitary stage inverter configuration with eight switches and three DC sources. A three stage multilevel inverter is gotten by interconnecting three single stage inverters to a star associated unadulterated resistive load with a typical earth point. Accordingly, this circuit offers lesser entryway control hardware, lesser cost, lesser warming, more ase of establishment and lesser electromagnetic interference.

Table I demonstrates the correlation of the quantity of components between diverse topologies. The execution of the inverter utilizing IPD, APD, CO and VF PWM techniques is indicated [8]. A passive arrangement LC channel is intended to create a sine wave from the staircase inverter yield. The motivation behind the output LC channel is lessening voltage swells because of the inverter switching [9]. This paper is sorted out into many segments. Segment II contains the circuit setup and its methods of operation. Section III says some balance plans accessible for switching of the inverter. The reenactment results are analysed in area IV. The waveform got subsequent to executing the series LC channel at the inverter yield is investigated in area V. Section VI gives the conclusion.
II. PROPOSED TOPOLOGY AND ITS OPERATION

The proposed inverter design has eight switches and three DC sources for every stage as appeared in Fig. 1. The arrangement mix among the three DC sources \( V_{dc} \), \( 2V_{dc} \) and \( 2V_{dc} \) can be utilized to produce eleven DC levels at the inverter yield in a solitary cycle. Fig. 2 gives the reenactment circuit of the proposed single stage circuit in MATLAB. In every mode, four of the switches work all the while.

![Proposed Configuration for Single Phase Inverter Operation](image)

III. MODULATION SCHEMES

To control the recurrence and music of the output voltage of the inverter, we should choose the most appropriate PWM procedure. The sinusoidal PWM (SPWM) technique has been connected to the power switches, in which a reference sinusoidal wave of major recurrence is contrasted with high frequency transporter wave(s). The level, recurrence or amplitude of the various bearer signs are fluctuated in view of the PWM technique. The tweak lists are kept same in all the methods for correlation. Abundancy regulation list is the ratio of the adequacy of the reference sine wave to the amplitude of the transporter waves. Recurrence balance index, is defined as the proportion of the recurrence of transporter wave to the frequency of the tweaking wave. Abundancy modulation index \( r_m \) and recurrence balance list \( m_r \) are given by (1) what’s more, individually.

\[
  r_m = \frac{A_m}{A_c} \quad (1)
\]

\[
  m_r = \frac{f_c}{f_m} \quad (2)
\]

The PWM strategies talked about in this paper are In Phase Disposition (IPD) sort level move beat width modulation (LS-PWM), Anti-Phase Disposition (APD) PWM Carrier Overlap (CO) PWM and Variable Frequency (VF)PWM. The abundancy tweak list \( r_m \) is kept up at 0.9 and the recurrence regulation file \( m_r \) at 200. The RMS value of the key part of the yield voltage and the add up to symphonious twisting (THD) are seen by using simulation comes about. In all the PWM systems, "N" number of carrier signs are utilized to acquire \( 2N+1 \) voltage levels.

A. In-Phase Disposition Level-Shift PWM (IPD-LSPWM) Method:
The transporter signals are level moved in this PWM technique. They have a similar plentifulness of 1 V and a frequency of 10kHz. The level moved transporter signals are compared with a diode connect corrected reference sine wave which is at principal recurrence, as represented in Fig.4. The different levels of the yield wave is identified and decoded to produce the beats required to trigger each switch in the inverter. Keeping in mind the end goal to acquire a three stage inverter, the sine wave is stage moved by 120°.

Fig.4. Reference Sine wave and Carrier waves for JPD-LSPWM at \( m_a = 0.9 \) and \( m_f = 200 \).

B. Against Phase Disposition Level-Shift PWM (APD-LSPWM) Method:

Every bearer flag is out of stage with neighbouring carrier motions by 180° and have a similar abundancy and frequency. The transporter signals are contrasted and the reference sine wave (which is at crucial recurrence) to produce required door beats as appeared in Fig.5.

Fig.5. Reference Sine wave and Carrier waves for APD-LSPWM at \( m_a = 0.9 \) and \( m_f = 200 \).

C. Bearer Overlap PWM (CO-PWM) Method:

This procedure uses level moved transporter rushes of the same recurrence and abundancy. They are in stage with one another and furthermore cover each other. They are contrasted with a diode connect redressed reference sine wave in Fig.6 all together to produce the entryway beats.

Fig.6. Reference Sine wave and Carrier waves for CO-PWM method at \( m_a = 0.9 \) and \( m_f = 200 \).

D. Variable Frequency PWM (VF-PWM) Method:

In Fig.7, all the level-moved bearer waves have the same amplitude. The lowermost bearer wave has exceptionally high frequency, 10kHz took after by 8kHz, 6kHz, 4kHz and the uppermost transporter flag has most minimal recurrence, 2kHz. They are compared with the reference sine wave with fundamental frequency to create required exchanging beats.

Fig.7. Reference Sine wave and Carrier waves for VF-PWM at \( m_a = 0.9 \)

IV. Recreation RESULTS and DISCUSSION

Different PWM methods are connected to the proposed three stage inverter topology at a similar sufficiency and frequency regulation records utilizing MATLAB/Simulink. A comparative review has been made between the RMS values of fundamental estimation of the yield voltage and the aggregate harmonic distortion for a solitary stage utilizing the Fast Fourier Transform (FFT) square. The circuit parameters utilized are: \( f_c = 10kHz \); \( f_m = 50Hz \); \( A_m = 4.5V \); \( A_f = 5V \). Star associated resistance stack (\( R = S_{On} \))The three stage yield voltage waveform got from IPD-LSPWM strategy is appeared in Fig.8. It has noteworthy 11th, 17th, 21st, 25th, 27th and 29th consonant values as given by its FFT examination in Fig.9. The basic estimation of output voltage is higher and the THD is lesser in the IPD sort LSPWM than the APD sort. The transporter waves are in stage with each other in the IPD sort, bringing about less mind boggling hardware.
Fig.5. Output voltage wave JormJor three phase II level inverter using iPDLSPWM technique.

Fig.9. FFT Analysis of the symphonious range Jor iPDL-LSPWM procedure

The yield voltage and the FFT investigation for APDLS PWM technique are appeared in Fig.10 and 11 respectively .The seventeenth, 21st, 23rd, 25th, 27th promotion 29th music are noteworthy.

Fig.10. Output voltage waveform for three phase 11 level Inverter using APDLS PWM technique.

Fig.11. FFT Analysis of the harmonic spectrum for APD-LSPWM technique

Fig.13 gives the FFT examination of the output voltage of CO-PWM technique is appeared in Fig 12. The third, 5th,7th and seventeenth sounds have higher vitality. The output produced by CO-PWM has most noteworthy THD of 54.80% and lowest RMS estimation of major yield voltage of 127V among the four techniques. This strategy produces beats that overlap each other. Thus, the resultant voltage waveform has very high THD, which is not near the sine wave. The carrier waves have bigger amplitudes than different PWM techniques. The FFT of the inverter yield voltage in Fig.14 from the VF-PWM technique is exhibited in Fig.15. The THD obtained through this technique is just 12.51%. The spectrum has more seventeenth, 37th and 39th symphonious energy .Different transporter frequencies are utilized as a part of this method ,resulting in use of more simple segments and large circuitry. The size and cost of the circuit can be decreased by opting for advanced heartbeat era, by utilizing a suitable microcontroller pack.

Fig.14. Output voltage waveform for three phase 11 level Inverter using VF-PWM technique.

Fig.15. FFT Analysis of the harmonic spectrum for VF-PWM technique

The execution investigation of the three stage inverter based on the THD of the yield voltage is given in Table.3.VF-PWM method was observed to give minimum harmonics in the yield voltage among the four sorts.

V. Yield AFTER USING A LC FILTER

A L-C channel is associated at the yield of the inverter to produce a sinusoidal waveform with lessened THD. The L and C qualities are intended to keep up the exchanging swell current under the objective esteem. The inductance esteem is along these lines given by:

\[
L \geq \frac{R_{L_{\text{max}}}}{3w} \quad \text{for single phase} \tag{3}
\]

\[
L \geq \frac{2R_{L_{\text{max}}}}{p(p^2-1)\omega} \quad \text{for polyphase} \tag{4}
\]

(\text{where } p=\text{number of phases and } w=21\text{f}). The three phase inverter is connected to a star connected pure resistance load.
of son. The capacitance value of the filter is assumed to be 1 \( \frac{1}{\text{IF}} \).

The signal obtained after the LC filter exhibits 1.77% THD. Fig. 17 provides the details of the harmonics of the output AC voltage waveform in Fig. 16.

VI. CONCLUSION

Three phase eleven level inverter topology with less number of switches is proposed and simulated. Various PWM methods are analyzed and compared. From the simulation results, it was found that VF-PWM provides minimum THD of 12.51% in the inverter output voltage. This will be the best PWM technique for inverter switching because small inductance can be used in the LC filter placed in series to the inverter output to produce a rectified AC sine wave of low THD of 1.77%.

REFERENCES